Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously Presented) An integrated tuner comprising: a step Automatic Gain Control (AGC) amplifier; and means for adjusting the step AGC amplifier (1) only during a vertical synchronization interval, wherein the adjusting means comprise: a clock generator for generating clock pulses; an up/down counter for generating control signals to adjust the step AGC amplifier; means for passing said clock pulses to said up/down counter only during said vertical synchronization interval.

3. (Previously Presented) An integrated tuner as claimed in claim 2, wherein the adjusting means further comprise: a level detector coupled to an output of the step AGC amplifier; and a dual comparator coupled to an output of said level detector to provide up/down control signals to said up/down counter in dependence on an output signal of said level detector.

4. (Previously Presented) An integrated tuner as claimed in claim 3, wherein the level detector continuously measures a total power of all signals in all channels applied to the step AGC amplifier.

5. (Canceled)

6. (Previously Presented) An integrated tuner comprising:

a step Automatic Gain Control (AGC) amplifier;

a synchronization slicer for separating a vertical synchronization signal from a Composite Video Broadcast Signal (CVBS) signal;

means for adjusting the step AGC amplifier only during a vertical synchronization interval output pulse period of the synchronization slicer;

wherein a width of the vertical synchronization signal output from the synchronization slicer is adjusted to control a number of pulses output to the means for adjusting the AGC amplifier.

7. (Previously Presented) An integrated tuner as claimed in claim 6, wherein the adjusting means comprise: a clock generator for generating clock pulses; an up/down counter for generating control signals to adjust the step AGC amplifier; means for passing said clock pulses to said up/down counter only during said vertical synchronization interval.

8. (Previously Presented) An integrated tuner as claimed in claim 7, wherein the adjusting means further comprise: a level detector coupled to an output of the step AGC amplifier; and a dual comparator coupled to an output of said level detector to provide

up/down control signals to said up/down counter in dependence on an output signal of said level detector.

9. (Previously Presented) An integrated tuner as claimed in claim 8, wherein the level detector continuously measures a total power of all signals in all channels applied to the step AGC amplifier.

10. (Previously Presented) A receiver comprising: an integrated tuner as claimed in claim 6; and an IF demodulation circuit for providing a vertical sync signal to the integrated tuner.

11. (Canceled)

12. (Previously Presented) An integrated circuit for a tuner application comprising the step AGC according to claim 2.